EEE/INSTR F313

Analog and Digital VLSI Design

BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI

ज्ञानं परमं बलम्

Analog VLSI Assignment

Name	ID No.
Sashank Krishna S	2019A8PS0184P
Anirudh Subramanian	2019A3PS0274P
Hariharan Venkat	2019A3PS0244P

Problem Number: 82

Acknowledgements

We would like to extend our deep gratitude to our Lecturers Dr. Anu Gupta and Dr. Samatha Benedict along with our tutorial instructors Dr. Satyendra Kumar Mourya and Dr. Karri Babu Ravi Teja for imparting the knowledge required for the completion of this assignment.

Problem Statement:

Question 82:

Design a low pass filter with cut-off frequency of 1MHz. Use a CMOS op-amp as shown in the question 77.

a) Analysis of all equations of your design, with a systematic derivation of all transistors' W/L ratios and simulation of circuits for the following specifications –
   i. Open loop gain (DC gain) >= 100dB
   ii. Phase Margin ≈ 45 degrees
   iii. Power dissipation <= 1mW
   iv. Slew rate >= 40V/microsecond

b) Show a biasing circuitry to bias all the voltages in your design (except the input)

c) Calculate and plot the following parameters for your Op-amp:
   i. DC gain
   ii. Bode Plot for AC gain and Phase
   iii. ICMR plot
   iv. Slew rate
   v. Differential Output voltage swing (dc + Transient)
   vi. Power Consumption
   vii. Input and Output offset voltage

Question 77:

Design a folded-cascode operational amplifier, in series-shunt feedback, with R-C frequency compensation for the following specifications:

a) Analysis of all equations of your design, with a systematic derivation of all transistors' W/L ratios and simulation circuit for the following specifications
   i. Voltage gain (closed Loop) >= 50
   ii. -3dB frequency >= 150MHz

b) Show a biasing circuitry to bias all the voltages in your design (except the input)

c) Calculate and plot the following parameters for your amplifier:
   i. Slew rate plot for step input of 1V
   ii. DC gain
   iii. Bode plot for AC gain and phase
   iv. ICMR plot
   v. Slew rate
   vi. Output voltage swing differential (dc + transient)
   vii. Power consumption
   viii. Input and output offset voltage

Introduction:

In analog electronics, a low pass filter is a filter that passes signals with a frequency lower than that of cutoff frequency and attenuates signals with frequencies higher than cutoff frequencies. Thus, a low pass filter will essentially ‘reject’ unwanted high frequencies and accept or pass only those lower frequencies that the designer of the circuit requires.
For low frequency applications, Passive low pass filters can be constructed using simple Resistance-Capacitance (RC) circuits, while higher frequencies usually require inductor components. Since such filters have no amplifying elements such as op-amps or transistors, they are usually called ***passive filters.***

By combining a basic RC low pass filter with an op-amp, we can construct an Active Low Pass Filter circuit that is simultaneously capable of amplification. In RC Passive first order filter circuits, the amplitude of the output signal is often much less than that of the input signal (i.e., gain<unity), and the load impedance affects the characteristics of the filter, in some cases, causing severe attenuation. To restore this loss of signal, we use ***active filters.***

Active Filters contain op-amps/transistors/FETs in the circuit design and use power from external sources to amplify the power at the output signal. Thus, we will be able to create a more selective output response, enabling the output bandwidth of the filter to become narrower or wider. An active filter will generally use an op-amp within its design which usually has a high input impedance, low output impedance and Voltage gain.

Design Process:

The design process started with the understand of the amplifier topology given to us. In the problem statement for question 82, we are directed to use the amplifier topology elucidated in question 77 which is the folded cascode. We thus started off with research pertaining to this new topology and it’s behavior. The circuit diagram we used for this purpose was found in [1] and is shown below.

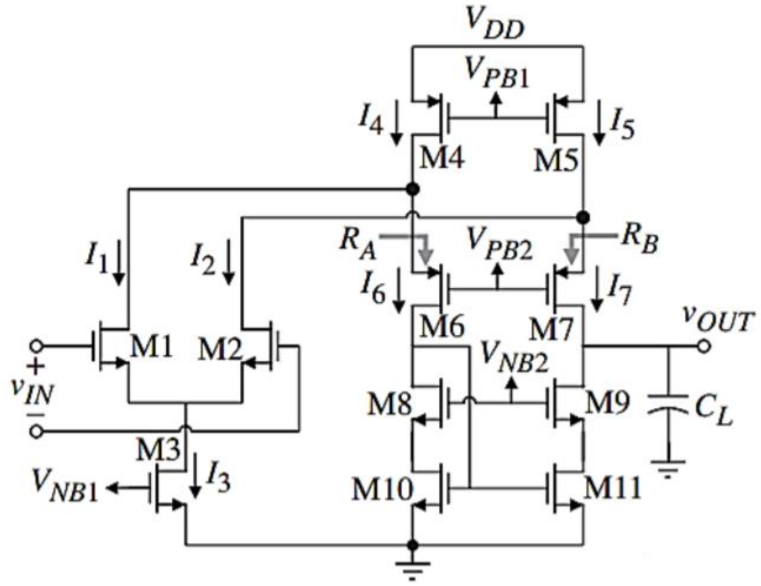
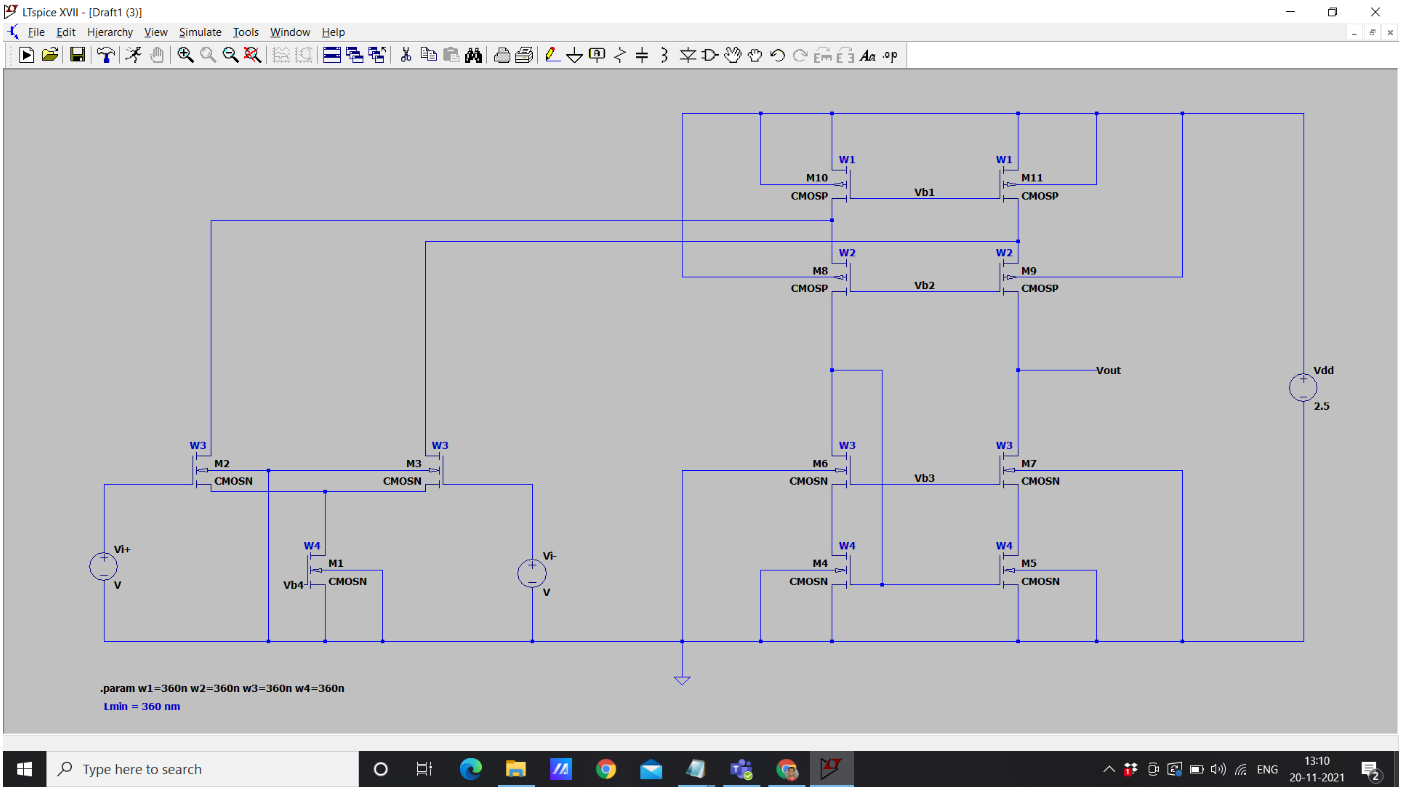


Fig 1: Circuit diagram of folded cascode amplifier topology

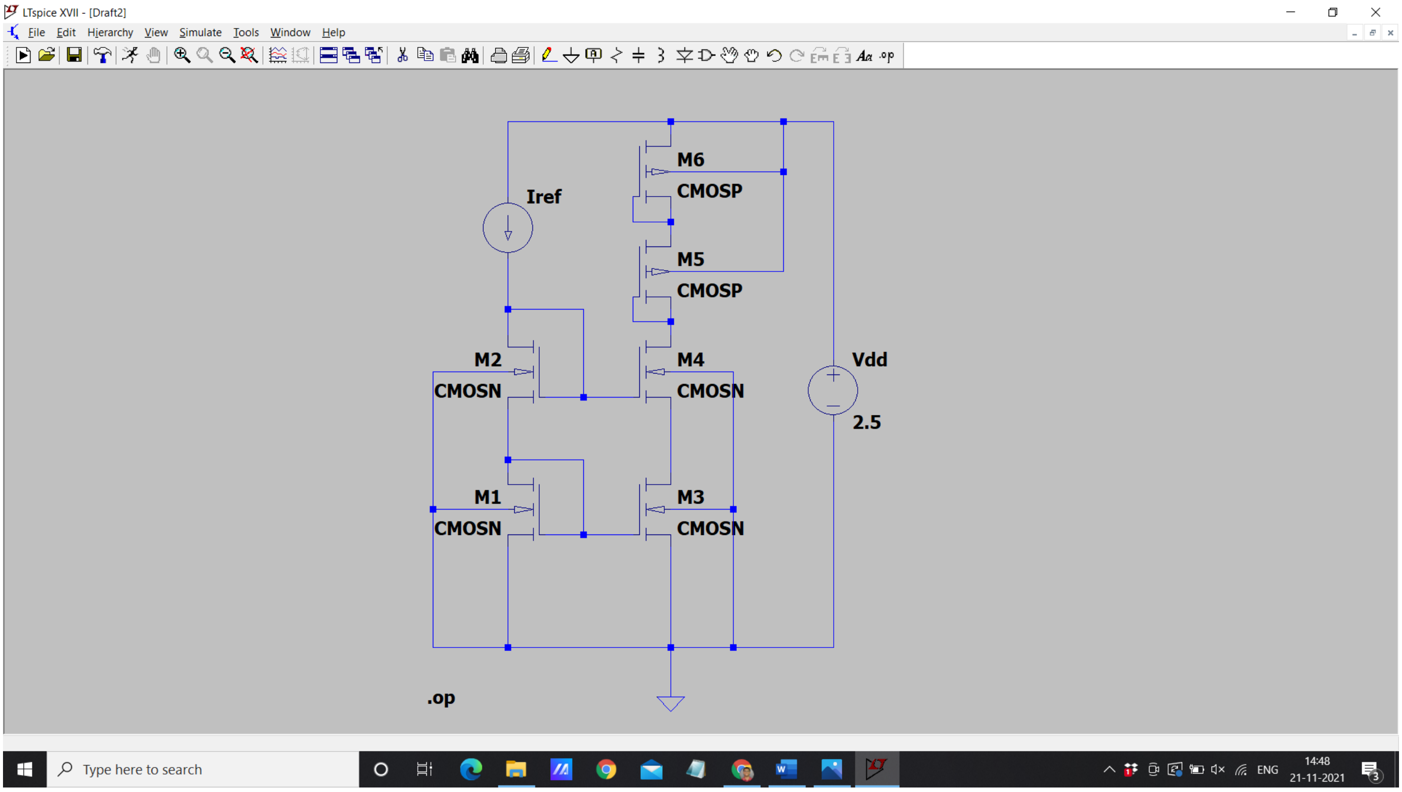
Once this information was gathered, the basic (unbiased) circuit diagram was made on the LTSpice simulation software. A V_{DD} = 2.5 V was taken and the models used for the PMOS and NMOS transistors were taken from the tsmc018.lib file as directed to us by the assignment sheet. The minimum channel length L_{min} was taken to be 360 nm as given in the assignment problem set. The load capacitor is not included in this schematic.



```
.param w1=360n w2=360n w3=360n w4=360n
Lmin = 360 nm
```

Fig 2: LTSpice schematic of unbiased folded cascode amplifier

After creating the basic circuit topology, it was time to bias the circuity in an effective manner. The following was the biasing circuity envisioned.



```
.op
```

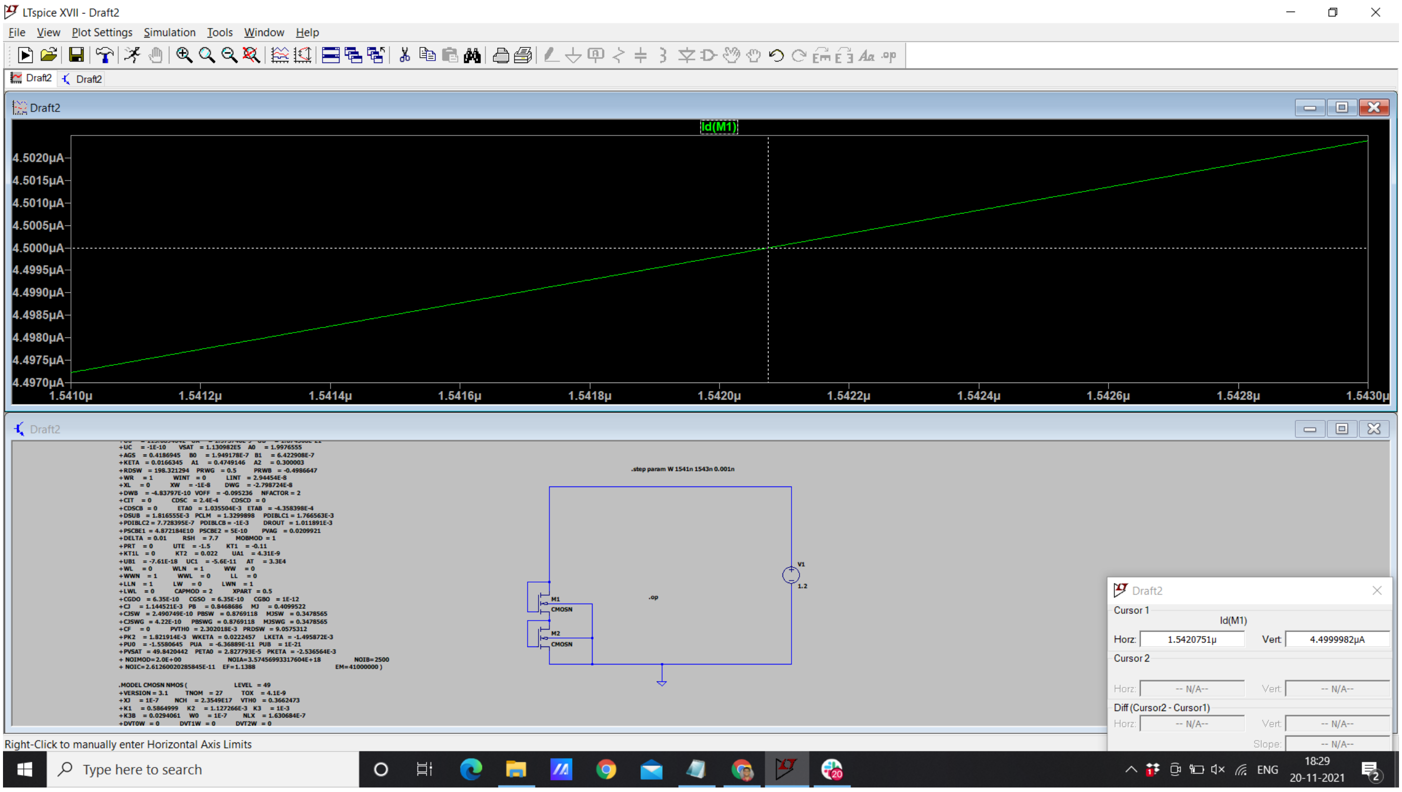
Fig 3: Biasing circuity topology used

The above topology was chosen after considering the instructions in the assignment which stated the use of a “Single ideal current source of arbitrary value with the positive node tied to V_{DD} or negative node tied to ground”. The above topology has the current source’s positive node tied to V_{DD} and thus satisfies the constraints given in the problem.

The next step was to decide on the value of current we will be using in the biasing circuity. For this purpose, we turned to running simulations on the above topology presented above. We first needed to decide on the potential drops across the P network and the N network. Their sum must be equal to V_{DD} which is 2.5 V. Due the PMOS being a weaker transistor, we allotted a drop of 1.3 V across the PMOS network and 1.2 V across the NMOS network.

Once this decision was made, simulations had to be run to see the current values which the networks were capable of handling. Since we knew the voltage drop across the network, we were able to parametrically sweep the W values of the transistors while plotting the current flow.

On analyzing the current characteristics, it was decided that a reference current of 4.5 μA was prudent. This was the case since very large W values were also not desired. The exact W values for the NMOS and PMOS transistors were found using the simulations.



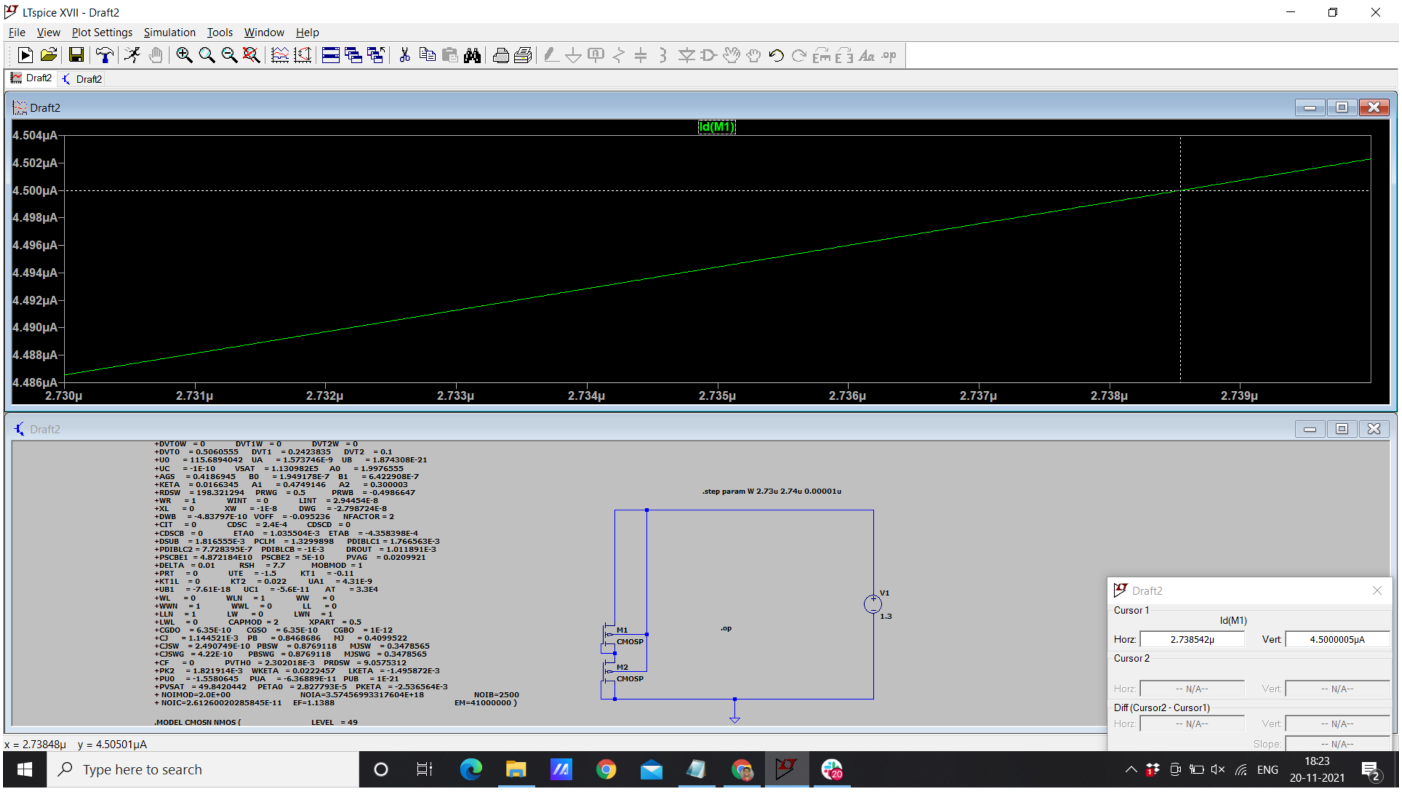
```
+UC    = -1E-10      VSAT   = 1.130982E5   A0    = 1.9976555
+AGS   = 0.4186945   B0     = 1.949178E-7  B1    = 6.422908E-7
+KETA  = 0.0166345   A1     = 0.4749146    A2    = 0.300003
+RDSW  = 198.321294  PRWG   = 0.5          PRWB  = -0.4986647
+WR    = 1           WINT   = 0            LINT  = 2.94454E-8
+XL    = 0           XW     = -1E-8        DWG   = -2.798724E-8
+DWB   = -4.83797E-10  VOFF  = -0.095236   NFACTOR = 2
+CIT   = 0           CDSC   = 2.4E-4       CDSCD = 0
+CDSCB = 0           ETA0   = 1.035504E-3  ETAB  = -4.358398E-4
+DSUB  = 1.816555E-3  PCLM  = 1.3299898    PDIBLC1 = 1.766563E-3
+PDIBLC2 = 7.728395E-7  PDIBLCB = -1E-3    DROUT = 1.011891E-3
+PSCBE1 = 4.872184E10  PSCBE2 = 5E-10      PVAG  = 0.0209921
+DELTA = 0.01        RSH    = 7.7          MOBMOD = 1
+PRT   = 0           UTE    = -1.5         KT1   = -0.11
+KT1L  = 0           KT2    = 0.022        UA1   = 4.31E-9
+UB1   = -7.61E-18   UC1    = -5.6E-11     AT    = 3.3E4
+WL    = 0           WLN    = 1            WW    = 0
+WWN   = 1           WWL    = 0            LL    = 0
+LLN   = 1           LW     = 0            LWN   = 1
+LWL   = 0           CAPMOD = 2            XPART = 0.5
+CGDO  = 6.35E-10    CGSO   = 6.35E-10     CGBO  = 1E-12
+CJ    = 1.144521E-3  PB    = 0.8468686    MJ    = 0.4099522
+CJSW  = 2.490749E-10  PBSW = 0.8769118    MJSW  = 0.3478565
+CJSWG = 4.22E-10    PBSWG  = 0.8769118    MJSWG = 0.3478565
+CF    = 0           PVTH0  = 2.302018E-3  PRDSW = 9.0575312
+PK2   = 1.821914E-3  WKETA = 0.0222457    LKETA = -1.495872E-3
+PU0   = -1.5580645  PUA    = -6.36889E-11  PUB  = 1E-21
+PVSAT = 49.8420442  PETA0  = 2.827793E-5  PKETA = -2.536564E-3
+ NOIMOD=2.0E+00               NOIA=3.57456993317604E+18          NOIB=2500
+ NOIC=2.61260020285845E-11   EF=1.1388                          EM=41000000 )

.MODEL CMOSN NMOS (                  LEVEL  = 49
+VERSION = 3.1       TNOM   = 27           TOX   = 4.1E-9
+XJ    = 1E-7        NCH    = 2.3549E17    VTH0  = 0.3662473
+K1    = 0.5864999   K2     = 1.127266E-3  K3    = 1E-3
+K3B   = 0.0294061   W0     = 1E-7         NLX   = 1.630684E-7
+DVT0W = 0           DVT1W  = 0            DVT2W = 0
```

```
.step param W 1541n 1543n 0.001n
```

Cursor 1
Id(M1)
Horz: 1.5420751µ Vert: 4.4999982µA
Cursor 2
Horz: -- N/A-- Vert: -- N/A--
Diff (Cursor2 - Cursor1)
Horz: -- N/A-- Vert: -- N/A--
Slope: -- N/A--

Fig 4: W value calculation for NMOS network

The thought process was to first create the part of the circuity which we wanted to test. In this case, it was the NMOS network in the biasing circuity. We know the total voltage drop across the network is 1.2 V. Using this information, we connect the circuity and run the simulation. Since we are looking to have 4.5 μA of current, we first run a simulation over a large range of W and then keep refining the search till the optimal precise W value is reached. For the NMOS network the W value obtained was Wnmos = 1542.0751 nm. A similar simulation was run for the PMOS network where the drop was 1.3 V (We get Wpmos = 2785.42nm).



```
+DVT0W   = 0          DVT1W   = 0          DVT2W   = 0
+DVT0    = 0.5060555    DVT1    = 0.2423835    DVT2    = 0.1
+U0      = 115.6894042  UA      = 1.573746E-9  UB      = 1.874308E-21
+UC      = -1E-10       VSAT    = 1.130982E5   A0      = 1.9976555
+AGS     = 0.4186945    B0      = 1.949178E-7  B1      = 6.422908E-7
+KETA    = 0.0166345    A1      = 0.4749146    A2      = 0.300003
+RDSW    = 198.321294   PRWG    = 0.5          PRWB    = -0.4986647
+WR      = 1            WINT    = 0            LINT    = 2.94454E-8
+XL      = 0            XW      = -1E-8        DWG     = -2.798724E-8
+DWB     = -4.83797E-10  VOFF    = -0.095236    NFACTOR = 2
+CIT     = 0            CDSC    = 2.4E-4       CDSCD   = 0
+CDSCB   = 0            ETA0    = 1.035504E-3  ETAB    = -4.358398E-4
+DSUB    = 1.816555E-3  PCLM    = 1.3299898    PDIBLC1 = 1.766563E-3
+PDIBLC2 = 7.728395E-7  PDIBLCB = -1E-3        DROUT   = 1.011891E-3
+PSCBE1  = 4.872184E10  PSCBE2  = 5E-10        PVAG    = 0.0209921
+DELTA   = 0.01         RSH     = 7.7          MOBMOD  = 1
+PRT     = 0            UTE     = -1.5         KT1     = -0.11
+KT1L    = 0            KT2     = 0.022        UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11     AT      = 3.3E4
+WL      = 0            WLN     = 1            WW      = 0
+WWN     = 1            WWL     = 0            LL      = 0
+LLN     = 1            LW      = 0            LWN     = 1
+LWL     = 0            CAPMOD  = 2            XPART   = 0.5
+CGDO    = 6.35E-10     CGSO    = 6.35E-10     CGBO    = 1E-12
+CJ      = 1.144521E-3  PB      = 0.8468686    MJ      = 0.4099522
+CJSW    = 2.490749E-10  PBSW    = 0.8769118    MJSW    = 0.3478565
+CJSWG   = 4.22E-10     PBSWG   = 0.8769118    MJSWG   = 0.3478565
+CF      = 0            PVTH0   = 2.302018E-3  PRDSW   = 9.0575312
+PK2     = 1.821914E-3  WKETA   = 0.0222457    LKETA   = -1.495872E-3
+PU0     = -1.5580645   PUA     = -6.36889E-11  PUB     = 1E-21
+PVSAT   = 49.8420442   PETA0   = 2.827793E-5  PKETA   = -2.536564E-3
+ NOIMOD=2.0E+00                 NOIA=3.57456993317604E+18            NOIB=2500
+ NOIC=2.61260020285845E-11   EF=1.1388                               EM=41000000 )

.MODEL CMOSN NMOS (                   LEVEL   = 49
```

```
.step param W 2.73u 2.74u 0.00001u
```

Draft2

Cursor 1

Id(M1)

Horz: 2.738542µ Vert: 4.5000005µA

Cursor 2

Horz: -- N/A-- Vert: -- N/A--

Diff (Cursor2 - Cursor1)

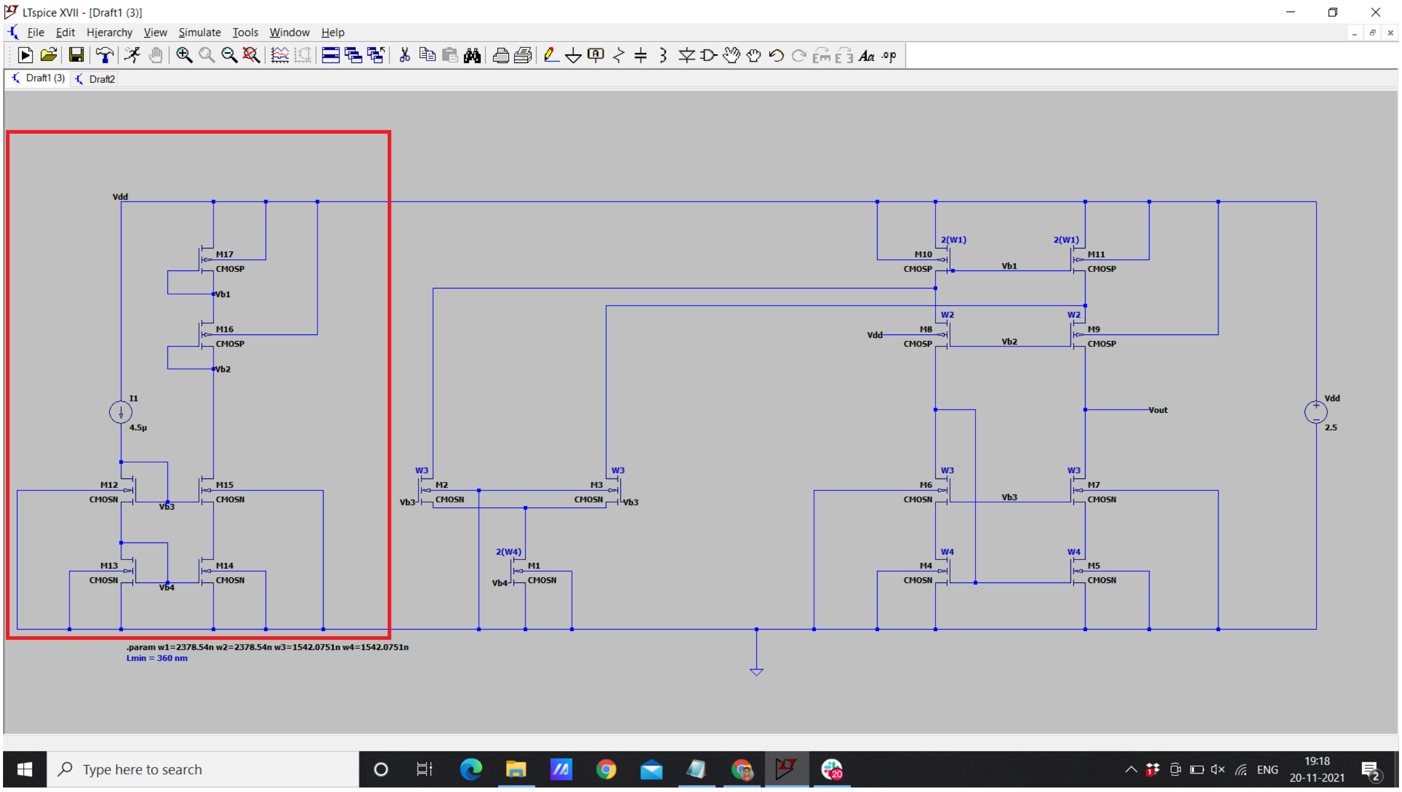
Horz: -- N/A-- Vert: -- N/A--

Slope: -- N/A--

x = 2.73848µ y = 4.50501µA

Fig 5: W value calculation for the PMOS network.

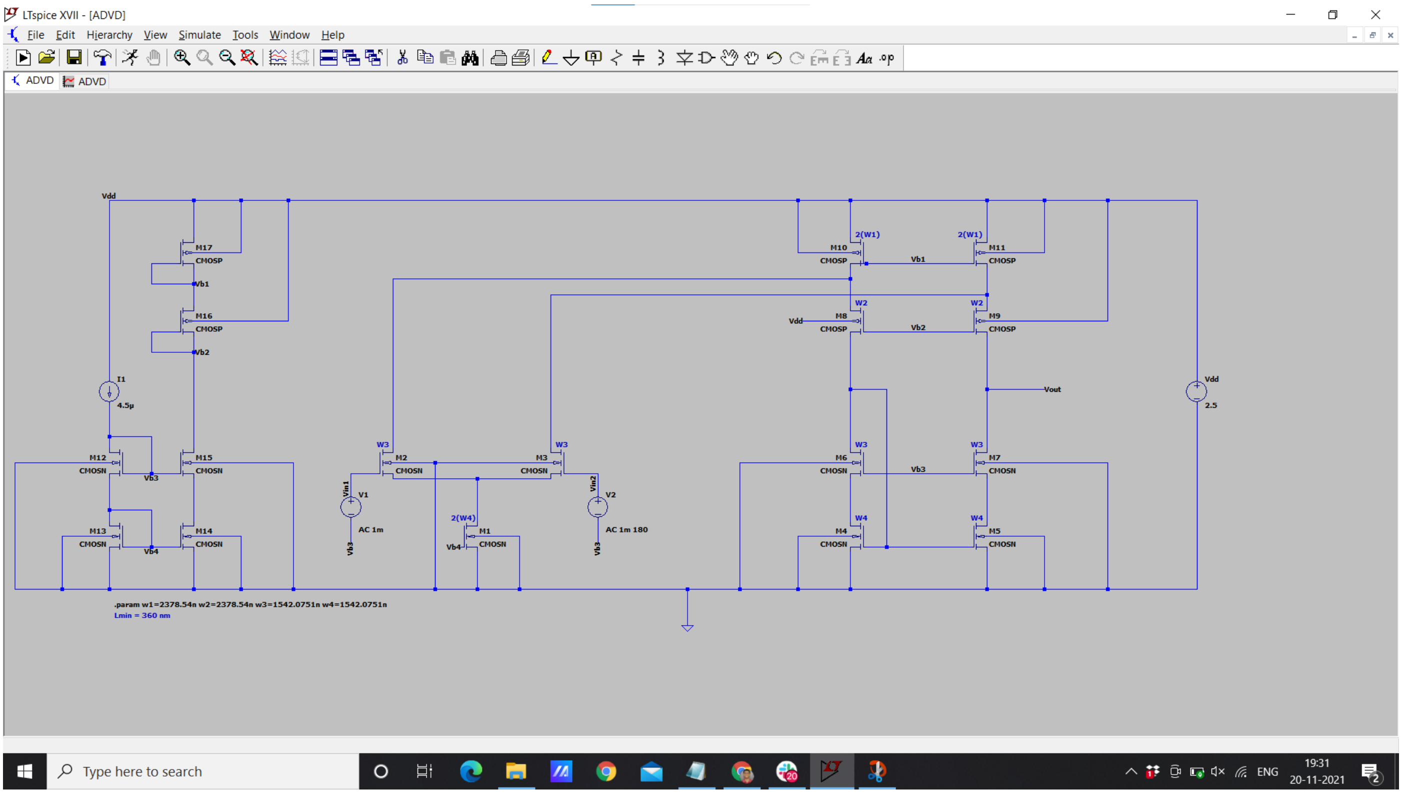
Once the current and width values for the biasing network was created, it was time for us to incorporate the biasing circuity into the amplifier topology. The figure below shows the complete biased amplifier schematic on LTSpice. The W values for all the other transistors in the main amplifier topology were decided with reference to the W values of the biasing network. The factors of '2' were included to allow for the necessary currents to be sinked or sourced at each node.



```
.param w1=2378.54n w2=2378.54n w3=1542.0751n w4=1542.0751n
Lmin = 360 nm
```

Fig 6: Complete biased amplifier (biasing circuitry shown in red)

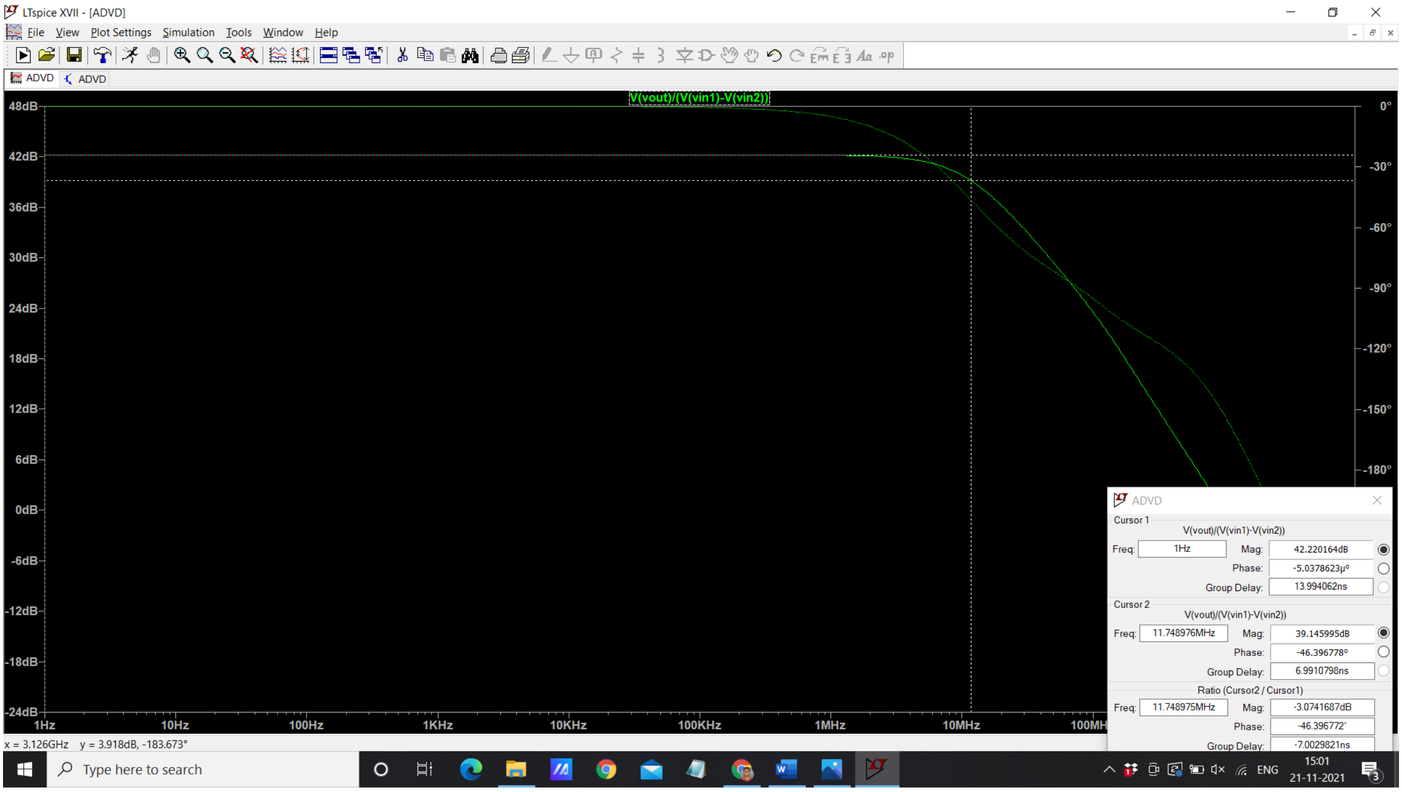
The important question of input bias needs to be addressed at this juncture. Using symmetry as the thumb rule, the input levels were given a DC bias of Vb3 as generated by the biasing circuity (this can be seen in Fig. 6 as well) and the AC small signals were riding on top of the mentioned DC shift. The “modified” AC analysis circuity is shown below.



```
.param w1=2378.54n w2=2378.54n w3=1542.0751n w4=1542.0751n
Lmin = 360 nm
```

Fig 7: AC operation of the amplifier

Now that the circuitry was AC operation ready, it was time to test the frequency response of the amplifier we had created. The Bode plot generated for the Version 1 open loop amplifier is shown below.



ADVD

Cursor 1

V(vout)/(V(vin1)-V(vin2))

Freq: 1Hz Mag: 42.220164dB ●

Phase: -5.0378623µ° ○

Group Delay: 13.994062ns ○

Cursor 2

V(vout)/(V(vin1)-V(vin2))

Freq: 11.748976MHz Mag: 39.145995dB ●

Phase: -46.396778° ○

Group Delay: 6.9910798ns ○

Ratio (Cursor2 / Cursor1)

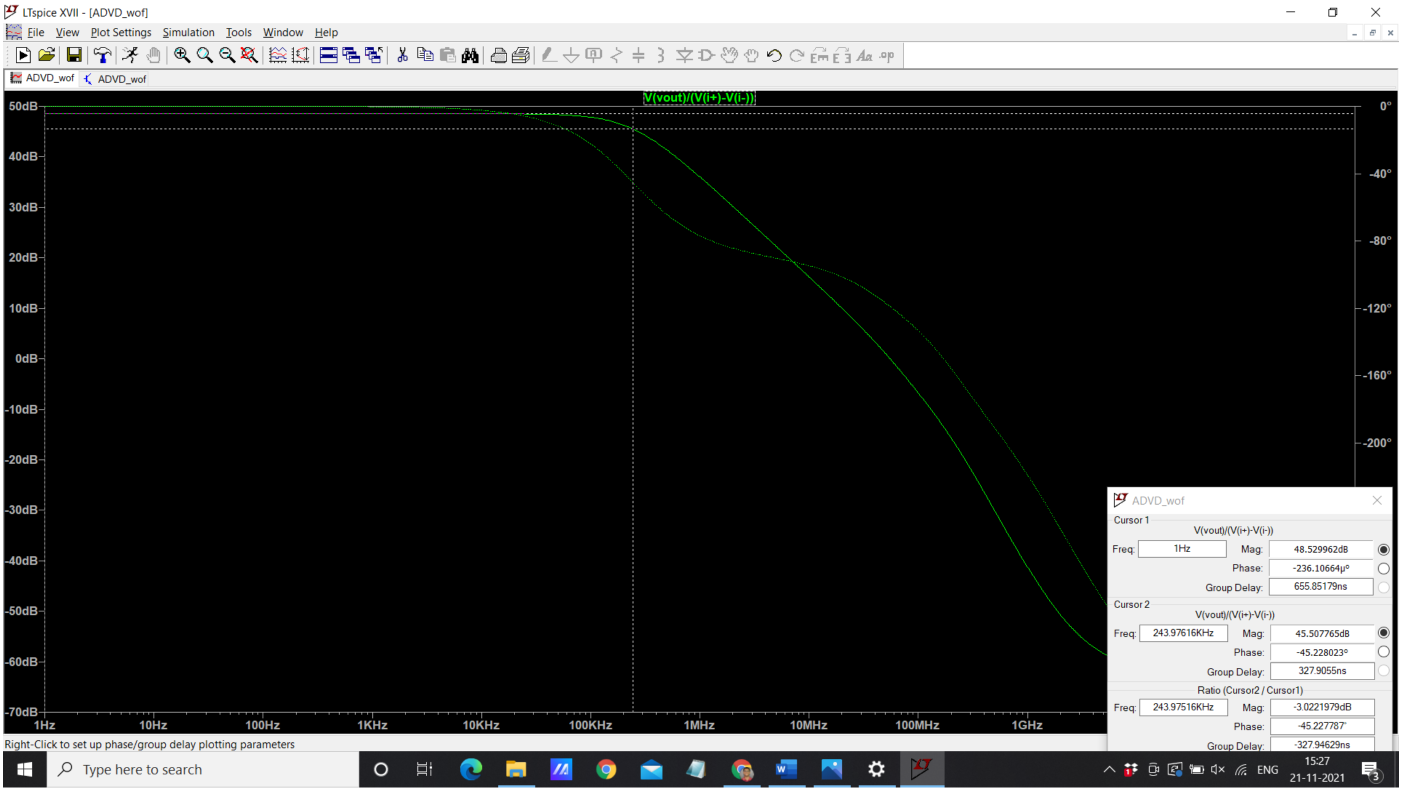
Freq: 11.748975MHz Mag: -3.0741687dB

Phase: -46.396772°

Group Delay: -7.0029821ns

Fig 8: Bode plot of amplifier (Version 1)

From the Bode plot, we see that we are getting around 42 dB of low frequency gain with a bandwidth of around 11 MHz. Before we move further, it is important for us to add in the load capacitance C_L. For reasons explained later, the C_L value was taken to be 150 fF which adheres to the >100 fF constraint imposed in the problem. The modified Bode plot after adding in the load capacitance is shown below.



ADVD_wof

Cursor 1
V(vout)/(V(i+)-V(i-))
Freq: 1Hz Mag: 48.529962dB ●
Phase: -236.10664µ° ○
Group Delay: 655.85179ns ○

Cursor 2
V(vout)/(V(i+)-V(i-))
Freq: 243.97616KHz Mag: 45.507765dB ●
Phase: -45.228023° ○
Group Delay: 327.9055ns ○

Ratio (Cursor2 / Cursor1)
Freq: 243.97516KHz Mag: -3.0221979dB
Phase: -45.227787°
Group Delay: -327.94629ns

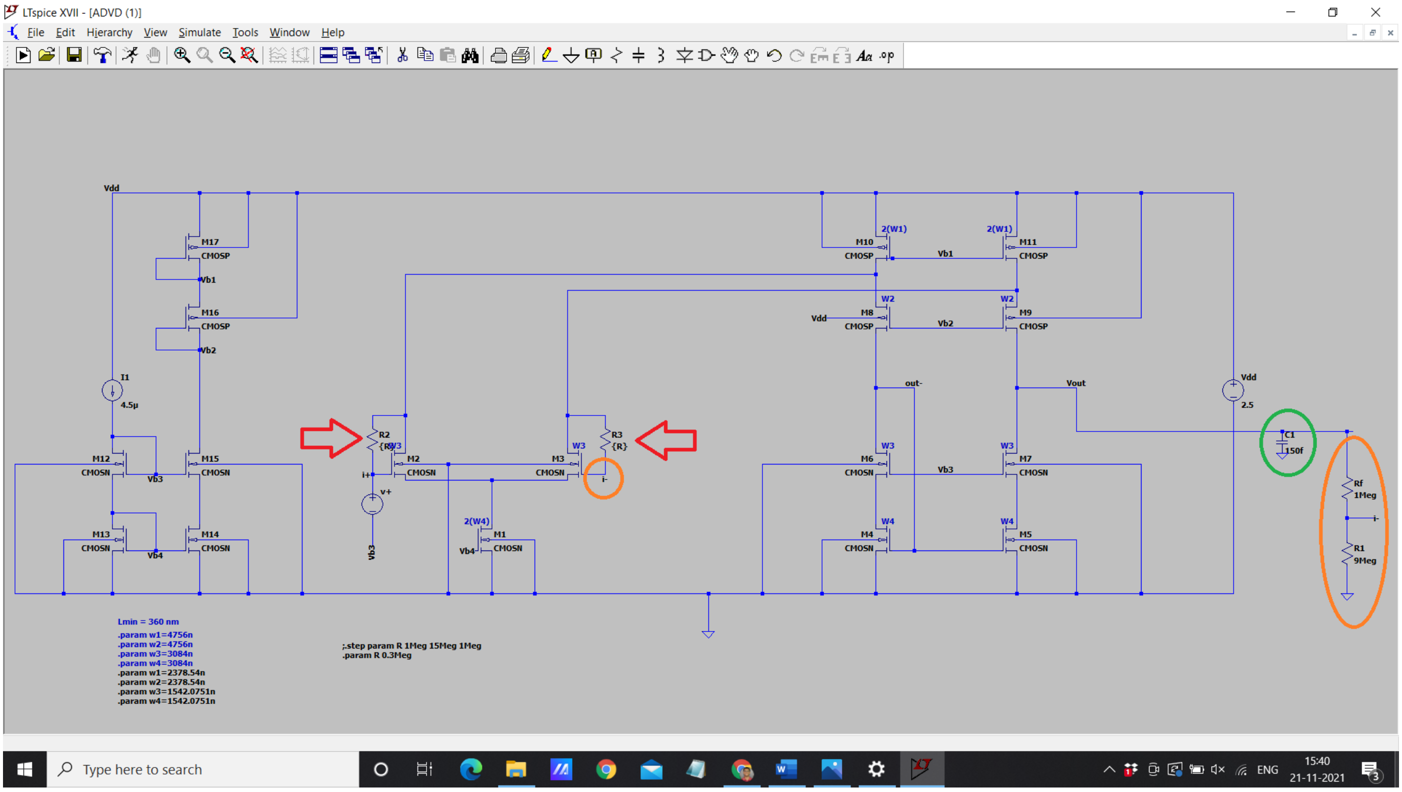
Fig 9: Bode plot after load capacitance of 150 fF was added at output

To our dismay, we notice the extremely poor bandwidth here of around 243 kHz which is much lower than the required value of 1 MHz. As a result, it is now time to implement the feedback and also incorporate frequency compensation to allow for a better frequency response.

It is important to note that the final circuit must be a feedback enabled low pass filter with a cutoff frequency of 1 MHz. While Problem 82 directs us to problem 77 for amplifier specifications, we note that the topology of the folded cascode is the most salient among those given specifications and try to optimize for the final goal at every stage.

As directed to us in the question, series-shunt feedback was incorporated using a resistive divider. Additionally, attempts were made to insert a “zero” into the frequency response of the amplifier, thereby increasing our bandwidth. The resistive components used for this purpose, along with the load capacitance C_L go hand in hand and need to be tweaked carefully.

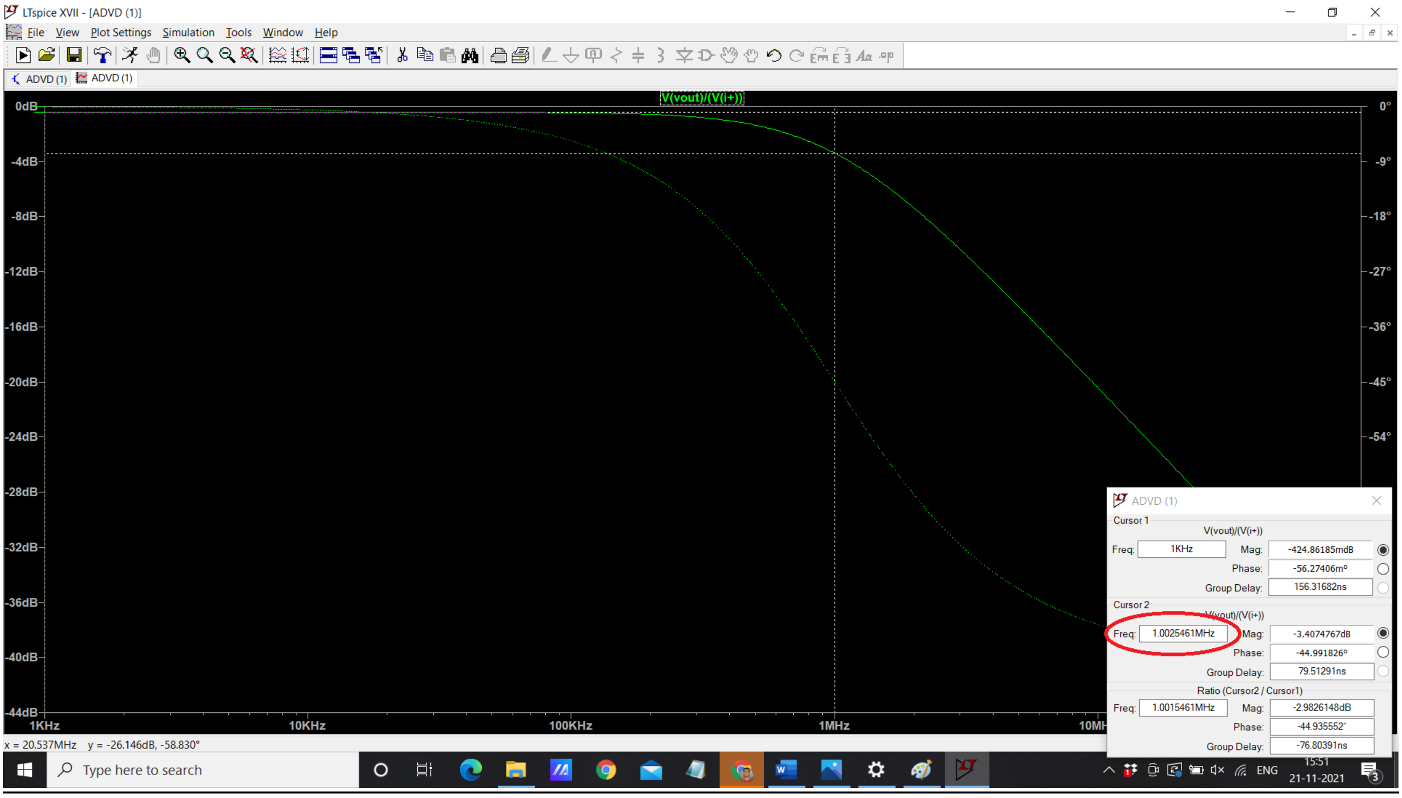
The final proposed schematic for the low pass filter, along with the Bode plot is showcased below. The diagrams are followed by the elaboration of the deliberations leading upto this schematic.



```
Lmin = 360 nm
.param w1=4756n
.param w2=4756n
.param w3=3084n
.param w4=3084n
.param w1=2378.54n
.param w2=2378.54n
.param w3=1542.0751n
.param w4=1542.0751n
```

```
;.step param R 1Meg 15Meg 1Meg
.param R 0.3Meg
```

Fig 10: Final schematic (feedback shown in orange, frequency compensation in red, and the load capacitance in green)



x = 20.537MHz y = -26.146dB, -58.830°

ADVD (1)

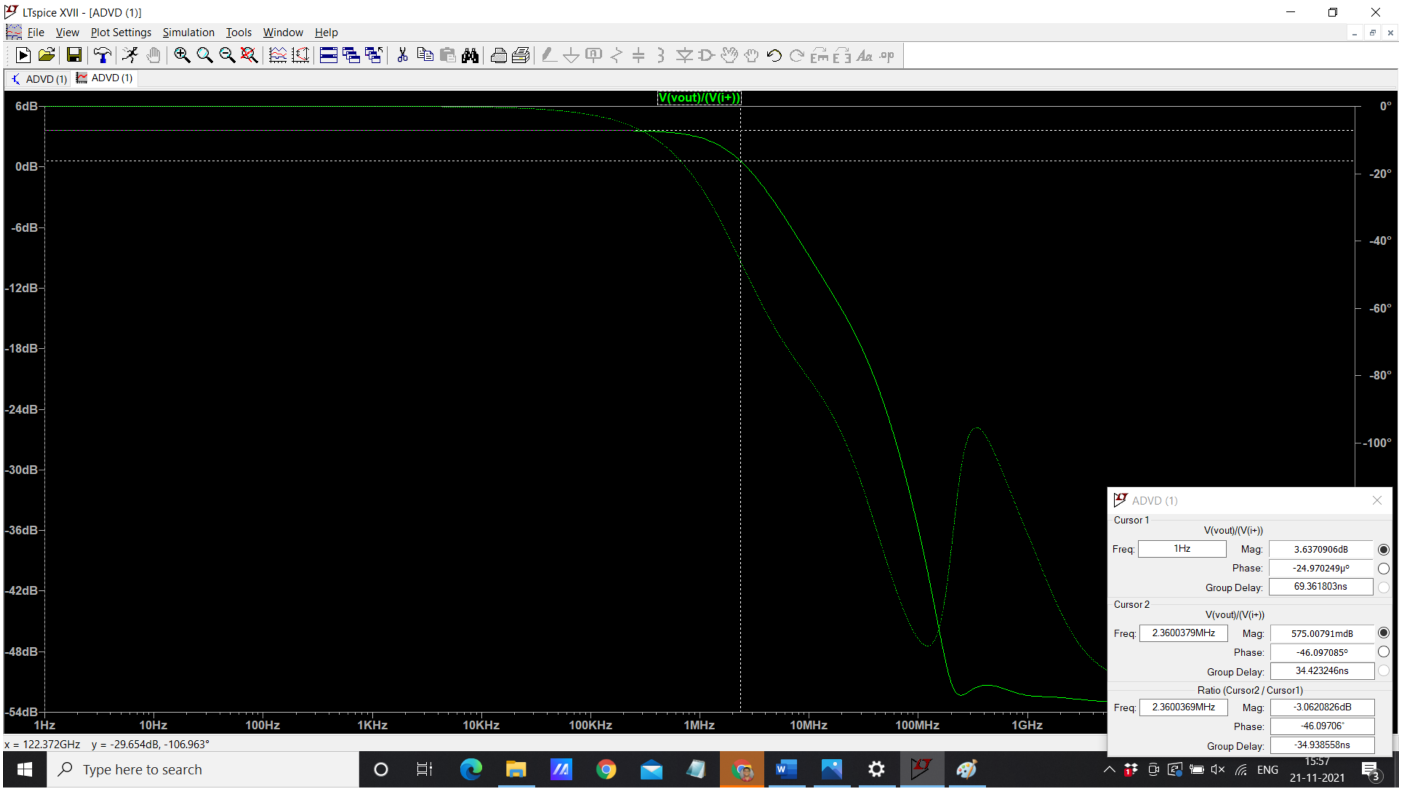
Cursor 1
V(vout)/(V(i+))
Freq: 1KHz Mag: -424.86185mdB
Phase: -56.27406m°
Group Delay: 156.31682ns

Cursor 2
V(vout)/(V(i+))
Freq: 1.0025461MHz Mag: -3.4074767dB
Phase: -44.991826°
Group Delay: 79.51291ns

Ratio (Cursor2 / Cursor1)
Freq: 1.0015461MHz Mag: -2.9826148dB
Phase: -44.935552°
Group Delay: -76.80391ns

Fig 11: Bode plot of final low pass filter. -3dB cutoff frequency highlighted in red

After careful deliberation, the value of R in the frequency compensation was chosen to be 300 kΩ. The thought process here is as follows. We can alter the bandwidth by changing the resistance and capacitance values. Increasing the resistance value allows for an increase in bandwidth. For example, a case where R = 1MΩ is shown below. The bandwidth for this case is almost double of the proposed solution.



ADVD (1)

Cursor 1

V(vout)/(V(i+))

Freq: 1Hz Mag: 3.6370906dB

Phase: -24.970249µ°

Group Delay: 69.361803ns

Cursor 2

V(vout)/(V(i+))

Freq: 2.3600379MHz Mag: 575.00791mdB

Phase: -46.097085°

Group Delay: 34.423246ns

Ratio (Cursor2 / Cursor1)

Freq: 2.3600369MHz Mag: -3.0620826dB

Phase: -46.09706°

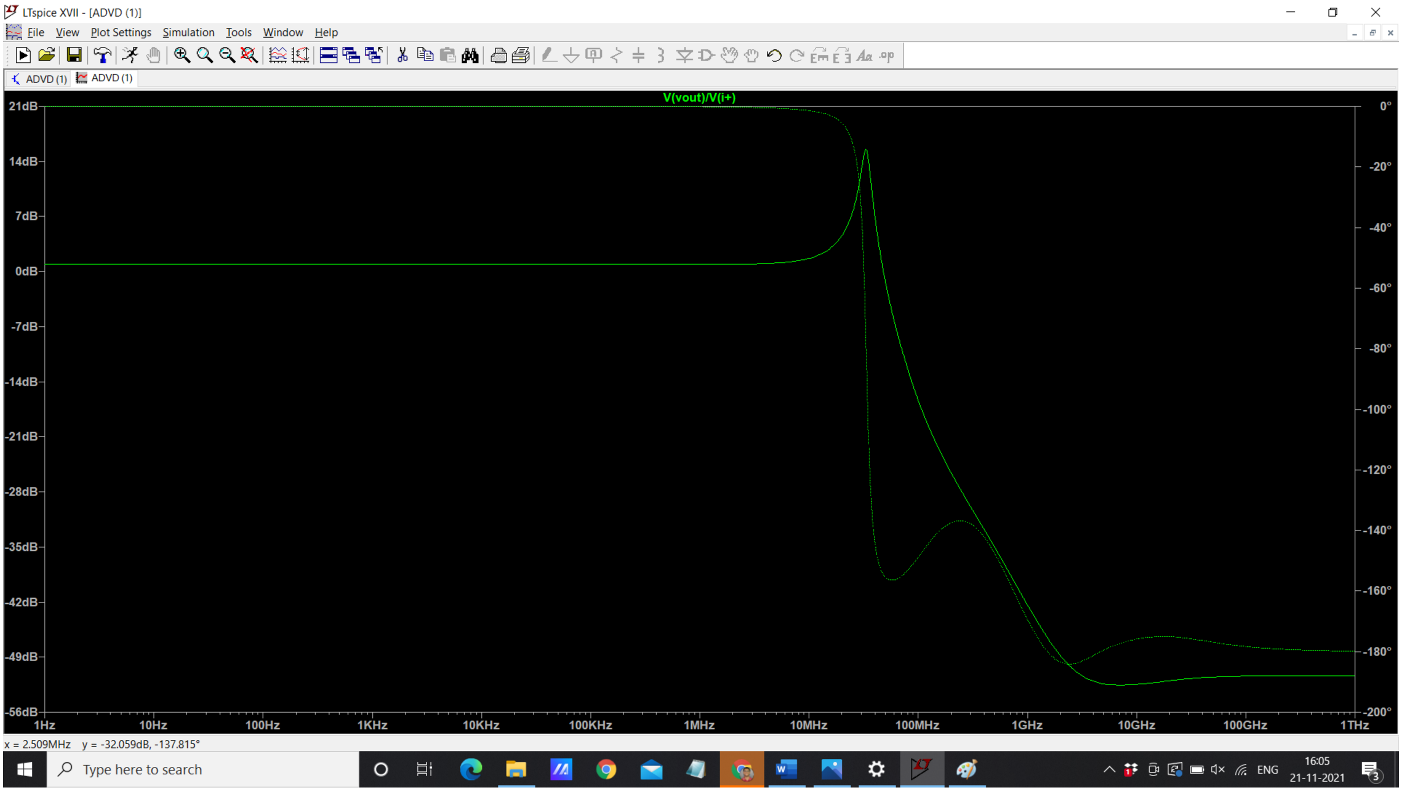
Group Delay: -34.938558ns

x = 122.372GHz y = -29.654dB, -106.963°

<u>Fig 12: Showing the increase in bandwidth for a higher R value (1MΩ)</u>

At the same time, as VLSI engineers, it is our duty to account for the Silicon areas. Having very high resistance nodes will imply more silicon area and will thus increase the costs. The value of 0.3 MΩ used in our proposed solution takes this into account and tries to use the minimum resistance while still meeting the minimum cutoff frequency requirement of 1 MHz.

One \interesting case we came across during our design process was the frequency response where we witnessed resonance firsthand before implementing frequency compensation. This problem is solved when the resistor for frequency compensation was added.



x = 2.509MHz y = -32.059dB, -137.815°

<u>Fig 13: Resonance observed when no compensation is used</u>

Final specification documentations:

V_{DD} = 2.5 Volts

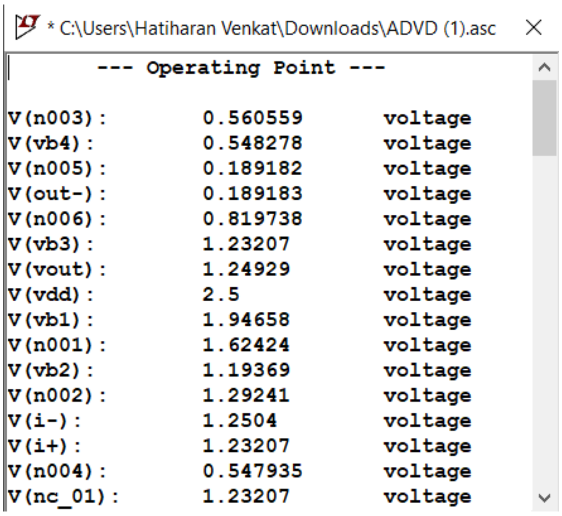
Simulations were run at 3 different temperatures of 0, 27 and 100°C. The results are tabulated below.

Property	**0℃**	**27℃**	**100℃**
Cutoff Frequency (MHz)	1.005	1.006	1.03
Power Dissipation (μW)	57.4866	56.8045	55.1318
DC gain (mdB)	-411.6981	-424.8581	-498.2211
Input DC bias (V)	1.22589	1.23207	1.25513
ICMR (V)	2.07	2.07	2.07

W/L Table (NMOS – green, PMOS – orange):

Transistor No.	**W (nm)**	**L (nm)**	**W/L**
M1	3084.1502	360	8.567
M2	1542.0751	360	4.284
M3	1542.0751	360	4.284
M4	1542.0751	360	4.284
M5	1542.0751	360	4.284
M6	1542.0751	360	4.284
M7	1542.0751	360	4.284
M8	2378.54	360	6.607
M9	2378.54	360	6.607
M10	4757.08	360	13.214
M11	4757.08	360	13.214
M12	1542.0751	360	4.284
M13	1542.0751	360	4.284
M14	1542.0751	360	4.284
M15	1542.0751	360	4.284
M16	4757.08	360	13.214
M17	2378.54	360	6.607

Voltages at all nodes:



```
       --- Operating Point ---

V(n003):        0.560559       voltage
V(vb4):         0.548278       voltage
V(n005):        0.189182       voltage
V(out-):        0.189183       voltage
V(n006):        0.819738       voltage
V(vb3):         1.23207        voltage
V(vout):        1.24929        voltage
V(vdd):         2.5            voltage
V(vb1):         1.94658        voltage
V(n001):        1.62424        voltage
V(vb2):         1.19369        voltage
V(n002):        1.29241        voltage
V(i-):          1.2504         voltage
V(i+):          1.23207        voltage
V(n004):        0.547935       voltage
V(nc_01):       1.23207        voltage
```

V_{DD} variation

The assignment instructed us to run the simulations at 10% higher and lower of V_{DD} with 0 degrees Celsius at 10% lower and 100 degrees Celsius at 10% higher. The results are tabulated below.

Property	**VDD = 2.25 V, T = 0℃**	**VDD = 2.75 V, T = 100℃**
Cutoff Frequency (MHz)	1.378	1.002
Power Dissipation (μW)	48.2	63.997898
DC gain (mdB)	-293.47365	-467.11457
Input DC bias (V)	1.217	1.263

References:

1. https://aip.scitation.org/doi/pdf/10.1063/1.5142133
2. https://www.electronicspoint.com/forums/resources/managing-temperature-in-ltspice.18/
3. https://www.youtube.com/watch?v=y31UMhCaTsY
4. https://www.youtube.com/watch?v=FxbnTWx8UZ0&t=4750s